

MARK S. HOFFMAN

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SUMMARY OF QUALIFICATIONS

Principal Design Engineer with four US patents and over 20 years of experience as project leader and individual contributor in system architecture, analog, digital, and power design. Detail-oriented, results focused team player with specific expertise in:

- Signal integrity
- Low noise.
- Power distribution
- Digital state machine design
- High speed timing analysis
- High current
- Heat removal and isolation
- HW/software/firmware trade-offs

Familiar with Cadence design entry, Allegro and Express PCB design, P-SPICE, H-SPICE, VB inside Excel.

PROFESSIONAL EXPERIENCE

Teradyne, Bedford and North Reading, MA

1998 – 2008

Principal Engineer in Hardware Design

Designed high speed digital and analog instruments.

Projects:

- Contributed and collaborated in developing Teradyne's highest selling system resulting in over \$1.25 billion sales.
- Designed new digital channel board (for two platforms) resulting in 100% speed increase..
- Designed the next generation digital channel board with twice the speed for two platforms.
- Redesign of 400MS/S source and 125MS/S (300MHz BW) digitizer to replace unreliable relays with FETs.

Accomplishments:

- Secured a strategic patent for creating a unique, inexpensive cooling technology that allowed reliable operation of a digital channel board.
- Created OptoFET model for P-SPICE that included parameters to control min/typ/max.
- Modeled attenuator using OptoFETs and found a way to match frequency response to 0.1 dB.
- Figured out a way to modify an FPGA to allow the old SW to work on the new architecture.
- MTBF improvement from 6,000 hours measured to 25,000 hours predicted.
- Acted as technical consultant and coordinated the work of various engineers on a project.
- Created Excel worksheet to estimate crosstalk from 4 3D analyses using Trend and SeriesSum functions.
- Modified web application to use more accurate formulas to calculate the characteristic impedance of PC stripes.
- Helped junior engineers understand principles of electronics and design trade-offs.

PictureTel, Andover, MA (bought by Polycom in 2000)

1992 – 1998

Testability Design Engineer

Advised system designers on ways to make product easier to test/debug.

Coordinated the development of checkers.

- Analyzed new designs for testability. Saved projected \$2M by improving one design.
- Wrote diagnostic tests for Network interface boards.
- Rewrote vendor's diagnostics to eliminate timing loops.
- Created a new way of injecting short delays in code.
- Wrote specification to allow vendors to modify their diagnostics to be run from our environment.
- Project manager: Technical supervisor of up to 6 people. Provided technical guidance, coordinated efforts, created schedules, reported progress to management.

OTHER RELATED WORK EXPERIENCE

- Awarded two patents in nV Measurement techniques
- Awarded a patent in Combinatorial Relay Multiplexing
- Designed 300 IC system controller/timing generator including ECL running at 100 MHz in a 100 IC synchronous state machine using VALID schematic capture, ABEL, and DATA I/O.
- Technical leader of team of four engineers.
- Designed backplane with controlled impedances, matched timing, and multiple power planes.
- Guided project from inception to product introduction well under scheduled time, including artwork, production, and test.
- Visited customer sites to solve technical problems and insure customer satisfaction.
- Designed special cable for high current references with 1/100 the inductance of the previous cable.
- Wrote internal article on designing backplanes for high current.
- Designed computer controlled 10A 25v programmable power supply with opto-coupled interface.
- Designed application packages for testing and automatically adjusting (using active laser trim) electronic ignitions (for General Motors and Chrysler) and electronically controlled wide angle tachometers.
- Corrected engineering design problems in a vendor supplied CRT and persuaded the manufacturer to implement most of them. Field failures per year improved to 5% from 30%.
- Worked on Electric Car project at Cornell. Won cross country race.

EDUCATION**BSEE**, Cornell University**MBA**, Boston University**PROFESSIONAL DEVELOPMENT**

Volunteer interpreter at Boston Museum of Science

Member IEEE

On the advisory board for the Harris Communications Group

Learned Cadence design entry, Allegro and ExpressPCB PCB design, P-SPICE, H-SPICE, VB inside Excel, Verilog, Xilinx, HTML/Java script.